AMENDMENTS TO THE SPECIFICATION:

Page 9; please amend the following paragraph after paragraph 0019:

FIGURE 4 illustrates a SRAM cell that is in accordance with ~~block diagram of an embodiment of a sleep mode voltage controller constructed according to~~ the principles of the present invention.

Page 18; please replace paragraphs 0034 and 0035 with the following amended paragraphs:

[0034] The third switch 230 may be controlled by a power-down signal PD that indicates when a SRAM array is entering the sleep mode. When in an active mode or standby mode, the power-down signal PD may be low and the third switch 230 is turned-on such that the high operating voltage V_{DD} is provided to the SRAM array. When entering the sleep mode, the power-down signal PD may go high and the third switch 230 is turned-off such that the high operating voltage V_{DD} is not provided to the SRAM array.

[0035] The first and second switches, 210, 220, may be controlled by a first and a second select signal SEL1, SEL2 that may be used to choose, adjust or refine the array high supply voltage V_{ADD} provided to the SRAM array by the sleep mode voltage controller 200. For example, the first select signal SEL1 may go low to turn on the first switch 210 when the power-down signal goes high. With the first switch 210 turned-on, a voltage drop across the first diode 250 may lower the high operating voltage V_{DD} and

provide the array high supply voltage V_{ADD} to the SRAM array. Additionally, the LDO 270 may regulate the array low supply voltage V_{ASS} provided to the SRAM array relative to the array high supply voltage V_{ADD}. Thus, the sleep mode voltage controller 200 may allow tight control of voltage across a SRAM cell which may be critical to stability while in the sleep mode.

Page 19, please replace paragraph 0036 with the following amended paragraph:

[0036] The second select signal SEL2 may be used to control the second switch 220 to adjust the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on parameters of the SRAM array transistors. Additional switches and diodes may also be included to allow additional adjustment or refinement of the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS}. One skilled in the art will also understand that the sleep mode voltage controller 200 may employ other components in addition to or instead of those illustrated to adjust and refine voltages provided to the SRAM array during the sleep mode.